WHAT IS CLAIMED IS:

1. A semiconductor memory device, comprising:

a memory cell array of dynamic memory cells;

an external access controller which outputs an external access execution timing signal for indicating an execution timing of an access operation to the memory cell array; and

a refresh controller which outputs a refresh execution timing signal for indicating an execution timing of a refreshing operation to the memory cell array, wherein

an output enable signal supplied from an external device changes to active in a read cycle;

a latch signal changes to active and then inactive to indicate latching of a read signal which is read from the memory cell array;

in the read cycle, the external access execution timing signal

changes to active triggered by the change of the output enable signal to active; and

changes to inactive triggered by a start of a latch of the read signal caused by changes of the latch signal to active and inactive;

a refresh requirement signal changes to active to instruct an execution of the refreshing operation to the memory cell array; and

in the read cycle, the refresh execution timing signal

changes to active according to the change of the latch signal to active while the refresh requirement signal is active; and

stays active for a predetermined time period.

2. The semiconductor memory device according to claim 1,

wherein

a write enable signal supplied from an external device changes to active in a write cycle;

in the write cycle, the refresh execution timing signal

changes to active according to a change of the write enable signal to active while the refresh requirement signal is active; and

stays active for the predetermined time period;

in the write cycle, the external access execution timing signal

changes to active according to a change of the refresh execution timing signal to inactive; and

changes to inactive according to the change of the write enable signal to inactive.

3. A semiconductor memory device, comprising:

a memory cell array of dynamic memory cells;

an external access controller which outputs an external access execution timing signal for indicating an execution timing of an access operation to the memory cell array; and

a refresh controller which outputs a refresh execution timing signal for indicating an execution timing of a refreshing operation to the memory cell array, wherein

an output enable signal supplied from an external device changes to active in a read cycle;

a latch signal changes to active and then inactive to indicate latching of a read signal which is read from the memory cell array;

in the read cycle, the external access execution timing signal

changes to active according to the change of the output enable signal to active; and

changes to inactive according to a start of a latch of the read signal after changes of the latch signal to active and inactive;

a refresh requirement signal changes to active to instruct an execution of the refreshing operation to the memory cell array; and

in the read cycle, the refresh execution timing signal

changes to active according to the change of the output enable signal to inactive while the refresh requirement signal is active; and

stays active for a predetermined time period.